WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first interconnect plane on a passivated substrate, the first interconnect plane being patterned and conductive,

a second interconnect plane separated from the first interconnect plane by a passivation layer, the second interconnect plane being patterned and conductive,

a conductive contact device selectively connecting the first and second interconnect planes,

a fuse device in a nonpassivated section of the second interconnect plane for selectively linking interconnects,

the fuse device being divided into fuse modules having fuse pairs that include fuse regions, the fuse regions being at a predetermined distance from one another, and selectively linked to a predetermined potential via a central interconnect.

2. The semiconductor device of claim 1, wherein said contact device is provided in a passivated section of the semiconductor device.

3. The semiconductor device of claim 1, wherein at least one of said fuse pairs extends at a right angle from said central interconnect.

4. The semiconductor device of claim 1, wherein at least one of said fuse pairs makes an acute angle relative to said central interconnect.

5. The semiconductor device of claim 1, further comprising:

a third interconnect plane between the passivated substrate and the first interconnect plane, the third interconnect plane being patterned and conductive.

6. The semiconductor device of claim 1, further comprising a latch adjoining said interconnect plane, and selectively connected to the predetermined potential via said fuse device.

7. A DRAM comprising a semiconductor device as recited in claim 1.

8. A DDR-DRAM comprising a semiconductor device as recited in claim 1.